REMARKS

This paper is responsive to the Office action dated January 18, 2005. Claims 1-88 were examined.

The Examiner's attention is drawn to a Preliminary Amendment mailed on June 4, 2004 (and received by the Office on June 8, 2004). That preliminary amendment provides application numbers unknown at filing and deletes unnecessary Attorney Docket Number references, and only touches the specification.

Specification

The specification was amended, as requested by the Examiner, to replace the numeral "106" with --406-- on page 34 at line 8. In addition, the following paragraph was also amended to correct a reference to the figure.

Claim Rejections – 35 U.S.C. § 112

Claims 6-11, 24-29, 42, 45, 68-72, 85, and 88 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 6, 24, and 68 have been amended to now recite "other associated array lines" in the second recitation of "associated array lines".

Claims 42, 45, 85, and 88 have been amended to provide clear antecedent support.

All issues raised by the Examiner have been addressed, and this rejection is believed to have been overcome.

Claim Rejections – 35 U.S.C. § 102

Claims 1, 3-5, 19, 42, 43, 45, 46, 48-52, 64, 85-86, and 88 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Derhacobian et al. (U. S. Patent No. 5,991,202). Applicant respectfully traverses this rejection in part.

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Regarding claims 1 and 46, the statement is made that Derhacobian et al. discloses "a memory array including memory cells (20, 30, 40) ..., said memory cells comprising modifiable conductance switch devices (30, 40)...". Applicant submits that transistors 30 and 40 are not memory cells, but rather select devices (a "select drain transistor 30" and a "select source transistor 40", per column 4, lines 1-3), although the devices labeled 20 are believed to comprise such memory cells.

Regarding claims 43 and 86, the statement is made that "transistors 30 and 40 in figure 2 of Derhacobian et al. have a charge storage dielectric as every other FET transistor." Applicant respectfully submits that (1) such transistors are not part of the memory cells; and (2) there is no disclosed charge storage dielectric for these transistors 30 and 40, nor for any other transistor described by Derhacobian et al. Applicant respectfully requests the rejection be withdrawn as to claims 43 and 86, which claims have been rewritten in independent form, and are believed allowable.

Regarding claim 51, the statement is made that Derhacobian et al. teaches "means (transistor 30 in unselected BL2) for coupling unselected NAND strings within a selected memory block to associated array lines (at both ends of the string) conveying an inhibit voltage (Vsupp) to establish a bias condition within such unselected NAND strings." Applicant respectfully disagrees. Derhacobian et al. describes (at column 4, lines 11-18):

> To program a selected cell S at the intersection of a selected bit line BL1 and a selected word line WL2 according to the methodology of the present invention, the unselected bit lines BL2-BLn *are first electrically isolated*, as in conventional programming techniques, by applying a supply voltage Vsupp, such as about 3 volts, to both the drain and the gate of their select drain transistors 30 *to turn the select drain transistors "off"*. Then a program voltage Vprog, such as about 18 volts, is applied to the selected word line WL2 ... *(emphasis added)*

Nowhere does Derhacobian et al. describe coupling unselected NAND strings within a selected memory block to associated array lines conveying an inhibit voltage to establish a bias condition within such unselected NAND strings, as recited in the claim. Rather, Derhacobian et al. describes *isolating* such unselected NAND strings as a first step in programming a selected memory cell. Applicant respectfully requests the rejection be withdrawn as to this claim. Claim 51 has been rewritten in independent form, and is therefore believed to be allowable.

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Claim 1 has been amended to include the limitation of allowable claim 41, and claim 46 has been amended to include the limitation of allowable claim 84. Thus, the rejection is believed to have been overcome as to these claims and any claims remaining dependent therefrom.

Allowable Subject Matter

Claims 2, 12-18, 20-23, 30-41, 44, 47, 53-67, 73-84, and 87 stand objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 6-11, 24-29, and 68-72 would likewise be allowable if rewritten to overcome the rejection under § 112 and to include all of the limitations of the base claim and any intervening claims.

Claims 6, 17, 18, 62, 63 have been rewritten in independent form.

Claims 19 and 41 have been amended to now depend from claim 6 rather than from claim 1. Claims 64 and 84 have been amended to now depend from claim 51 rather than from claim 46. All dependent claims are believed to be allowable at least for their dependence from an allowable independent claim.

Summary

In summary, claims 1-88 remain in the case. All claims are believed to be allowable over the art of record, and a Notice of Allowance to that effect is respectfully solicited.

Should any issues remain, Applicant respectfully requests a telephonic interview with the Examiner to discuss this response, and further in the hope that the remaining issues might be efficiently resolved.

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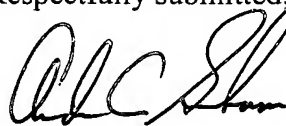I hereby certify that, on the date shown below, this correspondence is being

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Respectfully submitted,

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